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SEMICONDUCTOR DAMASCENE TRENCH AND METHODS THEREOF

BACKGROUND OF THE INVENTION

The present invention relates in general to the fabrication of integrated circuits, and in particular to integrated circuit structures having damascene trench gates and local interconnects formed in a single process, and methods of fabricating such integrated circuit structures.

Integrated circuit manufacturers continually strive to scale down semiconductor devices in integrated circuit chips. By scaling down semiconductor devices, greater speed and capacity can be realized while reducing power consumption of the chip. For example, in order to provide increased capacity in memory chips such as SRAM, it is highly desirable to shrink the size of each memory cell as much as possible without significantly affecting performance. This can be accomplished by shrinking the size of each component that forms each memory cell, packing the components closer together, or both.

Further, as integrated circuits are scaled down, the complexity of fabricating the components that make up the devices continues to increase. With the increase in complexity also comes an increase in the cost of fabricating the integrated circuits. For example, as memory cells in SRAM continue to shrink, undesirable variations between desired results and actual results become a limiting factor because of the inherent limitations in many processes employed in the course of manufacturing. For example, precision limits in photolithography, and deposition processes affect production parameters.

Also, every masking step that is performed during fabrication dramatically increases the cost of manufacturing a given device. For example, in a typical damascene gate structure, three or more deposition and planarizing steps are required.

Therefore, there is a continuing need for a structure, process and method of fabrication that allows consistent and reliable formation of damascene gates and interconnects using minimal manufacturing processes.

SUMMARY OF THE INVENTION

The present invention overcomes the disadvantages of previously known integrated circuit fabrication techniques by providing a structure, layout, and method thereof, that combines the formation of a damascene gate and damascene local interconnect into a single mask and process. By combining the formation of a damascene gate and local interconnect into a single process, the advantages of low resistance wordlines and reduced gate length are realized while eliminating the local interconnect to gate contact resistance. Further, the present invention provides flexible layout of active area to form small memory cells viable in a production environment. As such, the present invention is particularly suited for the fabrication of SRAM memory devices.

In accordance with one embodiment of the present invention, isolation trenches are formed in a base substrate. An ILD layer is deposited over the base substrate, then a patterning and etching process is performed to define gate/local interconnect damascene trenches. Any residual resist material is then stripped away. A layer of gate oxide is formed at least within the gate/local interconnect damascene trenches at areas where gates are to be formed. If oxide is formed on the base substrate in the contact areas that define local interconnects, a patterned oxide etch is performed to remove at least a portion of the oxide from the base substrate contact area within the gate/local interconnect damascene trenches in the areas to define local interconnects. Any desired implants are performed and any residual resist is stripped.

A conductive layer is deposited over the structure filling the damascene trenches thus defining damascene gates and local interconnects. A polishing process is then performed to polish back the conductive layer to the ILD layer. Next, the ILD layer is stripped and spacers are formed adjacent to the gates and local interconnects. After forming the spacers, any additional required doping is performed. For example, the base substrate is doped to define source and drain regions of active area. Finally, any required back end of line wiring is completed.

It is an object of the present invention to provide a semiconductor structure that requires only one deposition and CMP process in forming a gate and local interconnect.

It is an object of the present invention to provide a semiconductor structure that eliminates the local interconnect to gate contact resistances.

It is an object of the present invention to provide a small cell layout for an SRAM memory cell.

Other objects of the present invention will be apparent in light of the description of the invention embodied herein.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The following detailed description of the preferred embodiments of the present invention can be best understood when read in conjunction with the following drawings, where like structure is indicated with like reference numerals, and in which:

Fig. 1 is an illustration of a semiconductor base substrate having an isolation trench formed therein according to one embodiment of the present invention

Fig. 2 is an illustration of a semiconductor structure during fabrication wherein an ILD layer is formed on the base substrate of Fig. 1 according to one embodiment of the present invention;

Fig. 3 is an illustration of a semiconductor structure during fabrication wherein a patterned mask is formed over the ILD layer of Fig. 2 according to one embodiment of the present invention;

Fig. 4 is an illustration of a semiconductor structure during fabrication wherein gate/local interconnect damascene trenches are formed through the ILD layer, and the patterned mask of Fig. 3 is stripped away according to one embodiment of the present invention;

Fig. 5 is an illustration of a semiconductor structure during fabrication wherein an oxide layer is grown on the exposed silicon of the base substrate in the areas not covered by the oxide within the isolation trench or ILD layer Fig. 4 according to one embodiment of the present invention;

Fig. 6 is an illustration of a semiconductor structure during fabrication wherein a photoresist layer is patterned over the semiconductor structure of Fig. 5, portions of the oxide layer are removed, and implants are performed into the base substrate according to one embodiment of the present invention;

Fig. 7 is an illustration of a semiconductor structure during fabrication wherein the photoresist layer of Fig. 6 is stripped away;

Fig. 8 is an illustration of a semiconductor structure during fabrication wherein a conductive layer is deposited over the semiconductor structure of Fig. 7 according to one embodiment of the present invention;

Fig. 9A is an illustration of a semiconductor structure during fabrication wherein the conductive layer of Fig. 8 is polished back so as to be substantially flush with the ILD layer according to one embodiment of the present invention;

Fig. 9B is an illustration of a semiconductor structure during fabrication similar to that illustrated in Fig. 9A, wherein the damascene gate conductive material comprises polysilicon and the structure further includes an optional silicide layer formed over the damascene gate polysilicon according to one embodiment of the present invention;

Fig. 10 is an illustration of a semiconductor structure during fabrication wherein the ILD layer of Fig. 9A is removed;

Fig .11 is an illustration of a semiconductor structure during fabrication wherein a spacer layer is deposited over the damascene gate, local interconnect, and base substrate according to one embodiment of the present invention;

Fig. 12A is an illustration of a semiconductor structure during fabrication wherein spacers are formed on the damascene gate and local interconnect structures of Fig. 11 and subsequent source/drain implants are performed according to one embodiment of the present invention;

Figs. 12B illustrates the formation of optional silicide layers over the damascene gate and within the local interconnect according to one embodiment of the present invention;

Fig. 13 is an illustration of a semiconductor structure during fabrication wherein dielectric layers are formed over the structure of Fig. 12A, according to one embodiment of the present invention;

Fig. 14 is a flow chart illustrating the steps of manufacturing a damascene gate and local interconnect according to one embodiment of the present invention;

Fig. 15 is a schematic of an SRAM memory cell according to one embodiment of the present invention;

Fig. 16 is a layout of the SRAM memory cell according to one embodiment of the present invention; and,

Fig. 17 is a block diagram of a computer system using an SRAM memory device according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration, and not by way of limitation, specific preferred embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention.

It shall be observed that the process steps and structures described herein do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with a variety of integrated circuit fabrication techniques, including those techniques currently used in the art. As such, commonly practiced process steps are included in the description herein only if those steps are necessary for an understanding of the present invention.

As used herein, the formation of a layer or region "over" a substrate or other layer refers to formation above, or in contact with, a surface of the substrate or layer. For example, where it is noted or recited that an insulating layer is formed over a substrate, it is contemplated that intervening structural layers may optionally be present between the insulating layer and the substrate.

Fabrication of a Gate and Local Interconnect Damascene Trench

As illustrated in Fig. 1, the semiconductor structure 10 comprises a base substrate 12 having an isolation trench 14 previously formed therein. The base substrate 12 is silicon or any other semiconductor material or combination of materials as is known in the art. For example, the substrate 12 can comprise gallium arsenide (GaAs) or other semiconductor materials such as InP, CdS, or CdTe. The isolation trench 14 defines an isolation region, and is formed using any available techniques including for example, shallow trench isolation (STI) methods. As illustrated, the isolation trench 14 includes first and second sidewalls 16, a trench floor 18 generally parallel to the surface 12A of the base substrate 12, rounded lower trench corners 20 and rounded upper trench corners 22. An optional first oxide layer 24 lines the isolation trench 14, and a first dielectric material 26 fills in the isolation trench 14. It will be appreciated that the isolation trench 14 may contain additional layers or have a different geometry depending upon the isolation characteristics desired.

Ideally, the upper portion 28 of the first dielectric material 26 is planar and generally parallel to the base substrate surface 12A. However, a small convex surface in the upper portion 28 of the first dielectric material 26 may result depending upon the isolation trench formation techniques used. For example, in STI, layers of oxide and nitride are deposited over the base substrate, and a mask is patterned over the nitride to define the isolation region (not shown). After etching and filling the isolation trench with the first dielectric material, the mask, nitride, and oxide layers are stripped from the base substrate. For example, a wet etch, such as a hot phosphoric acid or other

suitable etchant is employed to remove the nitride layer and first dielectric layer generally above the isolation trench. However, the nitride layer may etch faster than the first dielectric material. As such, after also removing the oxide, such as with a buffered oxide etch (BOE), the convex surface on the upper portion 28 of the first dielectric material 26 is left as illustrated in Fig. 1. Such a construction generally will not affect the present invention, however it is undesirable to form a dish or divot in the first dielectric material 26 over the isolation trench 14 due to device performance limitations.

Typically, ions are implanted in the base substrate 12 to form n-type and p-type wells. This process is preferably performed after forming the isolation trench 14, but may be performed prior thereto. The wells define the locations of the n-channel and/or p-channel devices, thus the precise implants will be application specific. For example, to form a p-well, the base substrate 12 is implanted with a p-type dopant including for example, trivalent elements such as boron. Likewise, to form an n-well, the base substrate 12 is implanted with an n-type dopant including for example, pentavalent elements such as phosphorous. Further, ion implants may be embedded into the base substrate 12 through the isolation trench opening formed in the base substrate 12 before filling the isolation trench with the dielectric material 26.

Referring to Fig. 2, an interlayer dielectric (ILD) layer 40 is deposited over the base substrate 12. The ILD layer 40 is shown substantially conformal, however, such is not a requirement to practice the present invention. As such, there is no need to CMP or otherwise planarized the top surface of the ILD layer 40. As used herein, a conformal layer is a layer having a generally uniform thickness that follows the contours of the underlying layers. The ILD layer 40 may be any dielectric material, the selection of which may be dependent upon subsequent processes and the intended application. Further, the thickness of the ILD layer 40 can vary depending upon the application. For example, where the ILD layer 40 forms a gate, the thickness of the ILD layer 40 affects the height of the conductive material used to form the gate as more fully described herein, and thus provides a manner to affect the electrical characteristics of the gate.

Referring to Fig. 3, a second mask layer 42 is deposited over the ILD layer 40 and patterned to define the desired openings in the ILD layer 40, such as damascene gate/ local interconnects, or other devices. The second mask 42 may comprise for example, a photo resist layer or other process.

As illustrated in Fig. 4, an etching process is performed to define gate/local interconnect damascene trenches 44, 46. While only two gate/local interconnect damascene trenches 44, 46 are shown, any number of gate/local interconnect damascene trenches may be formed. Further, any combination of gates and local interconnects can be formed within each of the gate/local interconnect damascene trenches 44, 46 as explained more fully herein. It will be appreciated that the gate/local interconnect damascene trenches 44, 46 are formed in a single mask and etch operation. This reduces the cost of manufacturing integrated circuits according to the present invention. The second mask 42 (not shown in Fig. 4) is then stripped off.

For illustrative purposes, Figs. 4-13 show the formation of both a gate and local interconnect. As will be seen, a gate is formed in the gate/local interconnect damascene trench 44 and a local interconnect is formed in the gate/local interconnect damascene trench 46.

Further, the gate/local interconnect damascene trench 46 is illustrated partially overlying a portion of the isolation trench 14. However, this is only illustrative of the possible formations according to the present invention. For example, the gate/local interconnect damascene trench 46 can be formed so as to avoid overlying a portion of the isolation trench 14.

As illustrated in Fig. 5, a gate oxide layer 50 is grown on the base substrate 12. The gate oxide layer 50 can be grown by thermal oxidation of the base substrate 12, or by other conventional techniques such as chemical vapor deposition (CVD). It will be

appreciated that when growing the gate oxide layer 50, the oxide will form on any exposed silicon surface. As such, it may be necessary to remove any undesired oxide that formed as a result of the process. As an example, oxide will grow on the base substrate 12 within the portions of the gate/local interconnect damascene trenches intended to form local connections as illustrated by the gate/local interconnect damascene trench 46.

As illustrated in Fig. 6, a third mask 60 is deposited over the structure 10 and patterned to etch away undesired portions of the gate oxide layer 50 to define an active area contact or exhumed contact 62 generally within the area defining the gate/local interconnect damascene trench 46. However, oxide may be removed from portions of the gate/local interconnect damascene trench 44 if local interconnects are also formed within the trench.

Further, optional contact implants 64 are formed in the plug area 66. The contact implant 64 is provided to keep the contact from shorting to the substrate. Further, according to one embodiment of the present invention, the contact implants 64 will merge with source/drain implants for device connection. Thus contact implants may be formed in either of the gate/local interconnect damascene trenches 44, 46 where an interconnect is formed. It will be appreciated that depending upon the application, either no implant, or alternative types of implants may also be used. For example, an implant with low ion energies may be used to construct a field threshold voltage (V_t) implant to improve electrical isolation between active areas separated by isolation trench and isolation regions because the implant results in a reduced doping profile, and thus reduced electrical field and reduced leakage. Other types of implants including threshold implants, graded channel implants, or any other punch through implants desired by the intended application may also be embedded into the base substrate 12. The resist, or mask 60 is then stripped off as illustrated in Fig. 7.

As illustrated in Fig. 8, a conductive layer 70 is deposited over the structure 10. The conductive layer 70 forms the gate conductor and local interconnect conductor. The conductive layer 70 comprises for example, a metal, alloy, metal-based material, polysilicon, or polysilicon based material.

As illustrated in Fig. 9A, the structure 10 is then planarized using CMP techniques for example. Subsequent to the planarizing process, the conductive layer 70 that filled the gate/local interconnect damascene trench 44 defines the gate conductor 72, and the conductive layer 70 that filled the gate/local interconnect damascene trench 46 defines a local interconnect conductor 74.

If the conductive layer 70 comprises a layer of polysilicon, a further doping operation is performed. For example, a conductive layer 70 comprising polysilicon is deposited using a CVD process to a thickness generally between 500 Angstroms and 3000 Angstroms. If it is desired to dope the polysilicon to an n-type, then a diffusion, ion implantation, or other process is performed to sufficiently dope the polysilicon with an n-type substance such as phosphorous. Likewise, if it is desirable to dope the polysilicon to a p-type, then a p-type material such as boron is implanted into the polysilicon. The polysilicon is then annealed.

Referring to Fig. 9B, if the conductive layer is a polysilicon, a silicide layer 71 is optionally formed. For example, if a silicide is desired over the damascene gate 90, a film, or transition material such as a Group VIA element (W or Mo for example), is deposited onto the polysilicon conductive layer 70. A subsequent anneal forms the silicide, and chemical etches remove the un-reacted, deposited film from the top of the ILD layer 40.

The ILD layer 40 is then stripped away, as illustrated in Fig. 10. An etch may be performed to remove the ILD layer 40 (not shown) leaving a damascene gate structure 90 and a local interconnect damascene structure 92.

At this point, any further doping that has not already been completed is performed. For example, it may be desirable to reduce channel resistance or increase speed parameters, thus an ion implant is used to form the optional lightly doped drain regions (LDD) 94.

Referring to Fig. 11, a spacer layer 100 is deposited over the structure 10. As illustrated, the spacer layer 100 is generally conformal. The spacer layer 100 comprises for example, a layer of oxide or nitride deposited using CVD at a thickness generally between 500-1000 Angstroms. Referring to Fig. 12A, portions of the spacer layer 100 are removed to define spacers 102 against the vertical walls of the damascene gate structure 90 and the damascene local interconnect structure 92. The spacers 102 may have a rounded or curved edge by etching all horizontally disposed regions of the spacer layer 100 (not shown) such as by applying a directed reactive ion beam downwardly onto the substrate 12. Such a process is anisotropic and thus material is removed substantially vertically. It shall be appreciated that other anisotropic etch processing techniques may also be used.

After the etch is complete, a further ion implantation is performed to define the doped regions 95. The ion implant is at a higher concentration and energy than the previous implant, thus the doped regions 95 are illustrated as having a deeper penetration into the base substrate adjacent to the portion of the LDD regions 94 underneath the spacers 102. The LDD regions 94 and the doped regions 95 jointly define the doped source/drain regions 96. It will be appreciated that depending upon the intended application, one or both of the implant steps may be eliminated from the manufacturing steps. It will further be appreciated that the source/drain regions96 may be implanted during other processing steps.

Further, where the conductive layer comprises a polysilicon, an optional silicide layer may be desirable. Referring to Fig. 12B, after the formation of the spacers 102

and further doping is performed to define the doped source/drain regions 96, the silicide layer 71, cobalt for example, is deposited over the structure 10. After a subsequent anneal process, $CoSi_x$ is formed on the polysilicon conductive layer 70 and active areas, including the doped source/drain regions 96. The silicide layer 71 serves to lower the resistance of the polysilicon conductive layer 70. Subsequent chemical etches remove the un-reacted film (cobalt) from the spacers 102 and other dielectrics.

Referring to Fig. 13, a dielectric layer 104 such as a conformal tetraethyloxysilicate (TEOS), oxide, or nitride layer is deposited over the structure 10. The dielectric layer 104 serves as a barrier layer for subsequent manufacturing processes. Further, a thick dielectric layer 106 is deposited over the dielectric layer 104. It shall be appreciated that additional processing steps may be performed to connect the damascene gate 90 and the local interconnect damascene 92 to additional layers of metallization. For example, the damascene gate 90 and/or the local interconnect damascene 92 may be connected to back end of line wiring (BEOL). The BEOL wiring completes the circuits designed within the integrated circuit device.

Referring to Fig. 14, a method of fabricating a semiconductor device according to one embodiment of the present invention is summarized. The method 150 comprises forming isolation trenches in the base substrate at block 152. An ILD layer is deposited over the base substrate at block 154, then a patterning and etching process is performed to define gate/local interconnect damascene trenches. Any residual resist material is then stripped at block 158. A layer of gate oxide is formed at least within the gate/local interconnect damascene trenches at areas where gates are to be formed at block 160. If oxide is formed on the base substrate in the areas that define local interconnects, a patterned oxide etch is performed to remove at least a portion of the oxide from the base substrate within the gate/local interconnect damascene trenches in the areas to define local interconnects at block 162. Any desired implants are deposited at block 164 and any residual resist is stripped at block 166. A conductive layer is then deposited forming the damascene gate and local interconnects within the

gate/local interconnect damascene trenches at block 168. A polishing process is performed to polish back the conductive layer to the ILD layer at block 170. Next, the ILD layer is stripped at block 172 and any required doping is performed, such as LDD doping forming source and drain regions of active area, and further, spacers are formed adjacent to the gates and local interconnects at block 174. Finally, any required back end of line wiring is completed at block 176.

The SRAM Memory Cell

Now described is an example of one of the numerous applications for the techniques and structures taught herein, and further demonstrates several key advantages of the present invention. The following discussion illustrates how the structures described with references to Figs. 1-13 are used to implement a memory cell schematically illustrated in Fig. 15.

Fig. 15 schematically illustrates a typical SRAM memory cell and Fig. 16 illustrates a layout for the SRAM memory cell of Fig. 15 constructed according to the techniques taught herein. As illustrated in Fig. 15, the SRAM memory cell 200 comprises a pair of inverters 202 and 204 that are cross-coupled to form a bi-stable flip-flop 206. The first inverter 202 comprises a first p-type transistor 208 having first and second source/drain regions 210, 212 and a gate 214, and a first n-type transistor 216 having first and second source/drain regions 218, 220 and a gate 222. The second inverter 204 comprises a second p-type transistor 224 having first and second source/drain regions 226, 228 and a gate 230, and a second n-type transistor 232 having first and second source/drain regions 234, 236 and a gate 238. The bi-stable flip-flop 206 is isolated from the bitline 240 by a first access transistor 242 having first and second source/drain regions 244, 246 and a gate 248.

Likewise, the bi-stable flip-flop 206 is isolated from a compliment bitline 250 by a second access transistor 252 having first and second source/drain regions 254, 256

and a gate 258. Both the first and second access transistors 242, 252 are controlled by a common wordline 255. The operation of SRAM memory is well known in the art and will not be discussed herein.

The schematic illustrated in Fig. 15 is presented to clarify the layout used to construct the SRAM memory cell according to techniques described in the present invention and illustrated in Fig. 16. It will be appreciated that Fig. 16 is not drawn to scale. Further certain proportions of Fig. 16 are exaggerated to facilitate an explanation of certain aspects of the present invention.

As illustrated in Fig. 16, the memory cell 200 comprises a first strip 268 and a second strip 274 coupled together by first, second, third, and fourth strips of active area 294. Everywhere the first and second strips 268, 274 cross the active area 294, either a transistor is formed (illustrated as a dashed box) or a contact is formed (illustrated as either a round or elliptical shape). The first and second strips 268, 274, and wordline 255 form conductive interconnects and may be fabricated as a damascene trenches as discussed with reference to Figs. 1-13.

The gate 214 of the first p-type transistor and the gate 222 of the first n-type transistor 216 are constructed as part of first strip 268 by building damascene gate structures such as the damascene gate structure 90 illustrated in Fig. 13. Referring back to Fig. 16, the first contact 270 and the second contact 272 are constructed as part of the first strip 268 by building damascene local interconnect structures such as the damascene local interconnect structure 92 as illustrated in Fig. 13. Likewise, the second p-type transistor 224 and the second n-type transistor 232 are constructed as part of the second strip 274 by building damascene gate structures such as the damascene gate structure 90 illustrated in Fig. 13.

Referring back to Fig. 16, the third and fourth contacts 276 and 278 are constructed as part of the second strip 274 by building damascene local interconnect

structures such as the damascene local interconnect structure 92 as illustrated in Fig. 13. The active areas 294 represent various dopings in the base substrate. For example, the active area 294 may comprise LDD regions 94 illustrated in Fig. 11, doping regions 95 illustrated in Fig. 12A-13, the doped source/drain regions 96 illustrated in Figs. 12A-13. Further, the active areas 294 may include implants such as the contact implants 64 illustrated in Figs. 6-13. The contact implants 64 prevent the active area contact from shorting to the base substrate. The contact implants 64 further merge with the doped source/drain regions for device connection.

It will be observed that the common wordline 255 is schematically illustrated in Fig. 15 as a single continuous wordline. However, as illustrated in the layout of Fig. 16, the wordline 255 is actually two separate wordlines 255. By providing two separate wordlines that carry the same signal, fabrication symmetry is more easily achieved. This also allows the pull down transistors to be fabricated substantially identically and allows greater cell stability.

Referring now to Fig. 15, connection points 260 and 262 are connected together to cumulatively couple the first p-type transistor gate 214, the first n-type transistor gate 222, the source/drain region 228 of the second p-type semiconductor 224, the source/drain region 234 of the second n-type transistor 232, and the source/drain region 254 of the second access transistor 252. Likewise, connection points 264 and 266 are connected together to cumulatively couple the source/drain region 212 of the first p-type transistor 208, the source/drain region 218 of the first n-type transistor 216, the source/drain region 244 of the first access transistor 242, the gate 230 of the second p-type transistor 224, and the gate 238 of the second n-type transistor 232.

Referring back to Fig. 16, these connections are formed according one embodiment of the present invention using only the damascene trenches or first and second strips 268, 274 and active areas 294. The first p-type transistor gate 214 and the first n-type transistor gate 222 are formed in the first strip 268. The source/drain

region 228 of the second p-type transistor 224 is coupled to the first strip 268 via the active area 294 and second contact 272. The source/drain region 234 of the second n-type transistor 232 is coupled to the first strip via the active area 294 and first contact 270. The source/drain region 254 of the second access transistor 252 is coupled to the first strip 268 via active area 294 to the second contact 272.

Likewise, the source/drain region 212 of the first p-type transistor 208 is coupled to the second strip 274 via active area 294 to the fourth contact 278. The source/drain region 218 of the first n-type transistor 216 is coupled to the second strip 274 via the active area 294 to the third contact 276. The source/drain region 244 of the first access transistor 242 is coupled to the second strip 274 via active area 294 to the third contact 276. The gate 230 of the second p-type transistor 224 and the gate 238 of the second n-type transistor 232 are formed in the second strip 274.

It will be appreciated that the second contact 272 must short the n-doped active area (source/drain region 254 of the second access transistor 258) to the p-doped active area (source/drain region 228 of the second p-type transistor 224). Likewise, the third contact 276 must short the n-doped active area (source/drain region 244 of the first access transistor 242) to the n-doped active area (source/drain region 218 of the first n-type transistor 216). Therefore, the second and third contacts 272, 276 are illustrated as an ellipse to differentiate them from the first and fourth contacts 270 and 278.

The memory cell illustrated with reference to Figs. 15 and 16 can be used to construct memory devices suitable for use with general computer systems as illustrated in Fig. 17. A general computer system 300 comprises a microprocessor or central processing unit 302, that communicates with input/output (I/O) devices 304, 306 over a bus 308. It will be appreciated that any number of I/O devices can be used, and the selection of I/O devices will depend upon the application for which the computer system 300 is intended. The computer system 300 also includes random access memory

(RAM) 310 and may include peripheral devices such as a floppy disk drive 312 and a compact disk (CD) ROM drive 314 which also communicate with CPU 302 over the bus 308.

The computer system 300 is exemplary of a digital device that includes memory devices. Other types of dedicated processing systems, including for example, radio systems, television systems, GPS receiver systems, telephones and telephone systems.

Utilizing the method of the present invention, the space occupied by the memory circuits, for example the RAM 310 can be reduced, thus reducing the size of the overall system. The reduced memory cell size of the memory cell 200 is realized by the layout of active area as described with reference to Figs. 15 and 16, and the structure of the damascene trenches including gate and local interconnect described with reference to Figs. 1-13. It must be noted that the exact architecture of the computer system 300 is not important and that any combination of computer compatible devices may be incorporated into the system.

Having described the invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from the scope of the invention defined in the appended claims.

What is claimed is: